REMARKS/ARGUMENTS

Applicant respectfully requests reconsideration of the application.

This paper responds to the Office Action of February 11, 2004. A Petition for Extension of Time extends the time to respond through July 12, 2004. Accordingly, this response is timely.

Claims 1-60, 63-116, and 119-133 are now pending. Claims 1, 4, 22, 37, 51, 61, 87, 94, 96, 104 and 113 are independent.

I. Claims 1, 4 and 37

Claim 4 is discussed at paragraph 12 of the Office Action.[1] Claim 4 recites as follows:

> 4. A method, comprising the steps of:
>
> executing instructions fetched from first and second regions of a memory of a computer, the instructions of the first and second regions being coded for execution by computers of first and second architectures or following first and second data storage conventions, respectively, the memory regions having associated first and second indicator elements, the indicator elements each having a value indicating the architecture or data storage convention under which instructions from the associated region are to be executed, the first architecture having a pre-defined, established definition, the computer providing a faithful implementation of the first architecture;
>
> when execution of the instruction data flows or transfers from the first region to the second, adapting the computer for execution in the second architecture or convention. when execution of the instruction data flows or transfers from the first region to the second, adapting the computer for execution in the second architecture or convention.

Goetz '913 does not provide a "faithful implementation" of either of his two architectures. For example, at col. 17, line 23-25, Goetz states that he "modifies the address translation mechanism used by both architectures." At col. 17, line 51, Goetz describes

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[1] Applicant notes that the Office Action only indicates column and line numbers of the references, but not the particular elements of the reference thought to correspond to specific claim elements. In many cases, this leaves considerable ambiguity in the Office Action. Applicant requests that any future Office Action specify elements by name (in addition to line number) to remove such ambiguity. The Examiner may wish to confer with Examiner Henry Tang, whose Actions are generally unambiguous in this respect. *See also* 37 C.F.R. § 1.104(c)(2) ("...the particular part relied on must be designated as nearly as practicable. The pertinence of each reference ... must be clearly explained..." – note the two separate requirements).

"limitations placed on the X86 mechanism." Thus, Goetz concedes that he does not provide a "faithful implementation" of either architecture.

Because Goetz does not provide a "faithful implementation" of either architecture, Goetz cannot guarantee that his computer will run pre-existing "off the shelf" software. Rather, to the degree of the difference, software would have to be specially written or specially compiled to run on Goetz' machine.

Claims 1 and 37 recite similar language, and are patentable for similar reasons.

II. Claim 22

Claim 22 is discussed at paragraph 52 of the Office Action. Claim 22 recites as follows:

> 22. A method, comprising the steps of:
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> executing instructions fetched from first and second regions of a memory of a computer, the instructions of the first and second regions being coded for execution by computers following first and second data storage conventions, the memory regions having associated first and second indicator elements, the indicator elements each having a value indicating the data storage convention under which instructions from the associated region are to be executed;
>
> recognizing when program execution has flowed or transferred from a region whose indicator element indicates the first data storage convention to a region whose indictor element indicates the second data storage convention, and in response to the recognition, altering the data storage content of the computer to create a program context under the second data storage convention that is logically equivalent to a pre-alteration program context under the first data storage convention.

Paragraph 52.4 compares the "the indicator elements each having a value indicating the data storage convention under which instructions from the associated region are to be executed" to Goetz, col. 17, lines 24-33. However, here, Goetz only teaches a P bit that indicates an instruction set. There is no indication that Goetz ever uses two different "data storage conventions" as recited in claim 22, let alone indicates them with any "indicator." Rather, it appears that Goetz (much like the Richter '684 reference previously at issue) changes "data storage conventions" so that the conventions of the two architectures match each other, at least at any critical points. For example, Goetz "completely replaces" the X86 page table format, in favor of his modified PowerPC page table format, col. 18, lines 63-64, precisely so that two different conventions do not conflict.

Because claim 22 recites a limitation absent from the references, claim 22 is patentable.

III. Claim 51

Claim 51 is discussed at paragraphs 29 and 30 of the Office Action. Claim 51 recites as follows:

> 51. A method, comprising:
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> storing instructions in pages of a computer memory managed by a virtual memory manager, the instruction data of the pages being coded for execution by, respectively, computers of two different architectures and/or under two different execution conventions;
>
> in association with pages of the memory, storing corresponding indicator elements indicating the architecture or convention in which the instructions of the pages are to be executed, the pages' indicator elements being stored in a table whose entries are indexed by physical page frame number;
>
> executing instructions from the pages in a common processor, the processor designed, responsive to the page indicator elements, to execute instructions in the architecture or under the convention indicated by the indicator element corresponding to the instruction's page.

Claim 51 recites that the pages' indicator elements are stored in a table whose entries are indexed by physical page frame number. In contrast, the Office Action points to a table whose entries are indexed based on the virtual page number (Goetz '913, col. 10, line 8). The "real address" discussed in line 21 is the "address of the page table" as a whole, not a "physical page frame number" used as an "index" to an "entry" as recited in claim 51.

Claim 51 recites a limitation absent from Goetz '913, and is therefore patentable over Goetz '913.

IV. Claim 63

Claim 63 is now rewritten into independent form, without amendment. Claim 63 is discussed at paragraphs 32 and 34 of the Office Action, and recites as follows:

> 63. A microprocessor chip, comprising:
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> an instruction unit, configured to fetch instructions from a memory managed by the virtual memory manager, and configured to execute instructions coded for first and second different computer architectures or coded to implement first and second different data storage conventions;
>
> the microprocessor chip being designed (a) to retrieve indicator elements stored in association with respective pages of the memory, each indicator element

indicating the architecture or convention in which the instructions of the page are to be executed, and (b) to recognize when instruction execution has flowed or transferred from a page of the first architecture or convention to a page of the second, as indicted by the respective associated indicator elements, and (c) to alter a processing mode of the instruction unit or a storage content of the memory to effect execution of instructions in accord with the indicator element associated with the page of the second architecture or convention;

wherein the indicator elements are stored in a table distinct from a primary address translation table used by a virtual memory manager, the indicator elements of the table being stored in association with respective pages of the memory.

The Office Action points to col. 14, lines 19-22 and 54-62, as showing that the "indicator elements" of the claim are "stored in a table distinct from a primary address translation table." The sections indicated by the Office Action mention several "tables," but the Office Action does not indicate which particular one of these tables is thought to be "pertinent." Without some indication of pertinence, no rejection is raised, 37 C.F.R. § 1.104(c)(2), and Applicant is unable to respond directly.

Applicant notes that Goetz stores his P bits "in each PowerPC page table entry" (col. 17, lines 29-30). Thus Goetz does not meet the limitation that the indicator elements be "stored in a table distinct from a primary address translation table." Claim 61 is patentable over Goetz '913.

V. Claim 87

Claim 87 is discussed at paragraph 100 of the Office Action. Claim 87 recites as follows:

87. A method, comprising the steps of:

executing a control-transfer instruction under a first execution context of a computer, the instruction being architecturally defined to transfer control directly to a destination instruction for execution in a second execution context of the computer;

before executing the destination instruction, altering the data storage content of the computer to establish a program context under the second execution context that is logically equivalent to the context of the computer as interpreted under the first execution context, the reconfiguring including at least one data movement operation not included in the architectural definition of the control-transfer instruction.

Claim 87 recites "executing a control-transfer instruction ... architecturally defined to transfer control directly to a destination instruction." The Office Action does not indicate which

of the three references is thought to teach the "control-transfer instruction" with the properties recited in claim 87. Thus no rejection is raised, and Applicant is unable to respond directly.

Applicant notes that Brender '422 is implemented entirely in software, by a special "jacket compiler" and linker. Brender '422, col. 10, lines 43-58. Brender specifically states that hardware for the new architecture is "not available." Col. 2, lines 59-60.

Further, Brender '422 teaches that the control transfer instruction must transfer control to the jacket, not "directly to a destination instruction" as recited in claim 87. Brender's linker recognizes when a call would cross from the X environment to the Y environment, and inserts a transition "jacket" between the two that effects the transition. Each "jacket" is particularly tailored to effect the transition from one source point to one destination, and another jacket is required for the return back. Brender '422, col. 10, line 64 to col. 11, line 14. Where the system cannot build a jacket automatically, the user must supply a custom-built software jacket. Col. 11, lines 15-22. Thus, there is never a "direct" control transfer, as recited in claim 87.

Murphy '947 apparently discusses the identical mechanism ("Jacketing System structure Produced at Compile Time," col. 5, line 29 to col. 7, line 40), and therefore similarly lacks the "direct" control transfer recited in claim 87.

Because no rejection has been raised, and all three of Goetz '913, Brender '422 and Murphy '947 lack the "instruction" recited in claim 87, claim 87 is patentable over these three references.

VI. Claim 94

To paraphrase claim 94, a control transfer may transfer to two different destinations, coded in two distinct instruction sets, without modification of the code between the two executions.

The Office Action discusses claim 94 at paragraphs 43-44, though it is not clear whether the comparison is made to Brender '422 or Murphy '947. In either event, it is clear that the Office Action misinterprets these two references. As noted in the above discussion of claim 87, Brender '422 is implemented entirely in software, and thus has no relevance to claim 94. At col. 10, lines 29-40, Brender '422 further distinguishes itself from claim 94, by noting that he

provides a customized "jacket" for each and every source/destination pair. Brender's jacket only works for that single transition. Thus, a transfer from SA to SB must go through an SA-SB jacket. If SA wants to transfer to SC instead of SB, SA must transfer to the SA-SC jacket, not the SA-SB jacket.

The two transfers recited in claim 94 cannot occur in Brender '422. Brender '422 must make each transition through a jacket that is particularized to that particular transition.

Claim 94 is patentable over Brender '422.

VII. Claim 96

Claim 96 is discussed at paragraph 100 of the Office Action. Paragraph 100 does not clearly indicate which of the three references is thought to correspond to which limitation of claim 96, and thus no rejection is raised, and Applicant is unable to respond directly.

As noted in the above discussion of claim 87, Brender '422 and Murphy '947 are entirely software based (see discussion of claim 87, above). Goetz '913 does not discuss differences in data storage convention (see discussion of claim 4). No combination of these three references could meet claim 96.

VIII. Claims 104 and 113

Claim 104 is discussed at paragraph 42 of the Office Action.

> 104 A method, comprising the steps of:
>
> executing instructions fetched from first, second and third regions of a single address space of the memory of a computer, the instructions of the first and second regions being coded for execution by computers of first and second architectures, the instructions of the second and third regions following first and second data storage conventions, respectively, the memory regions having associated modifiable indicator elements, a hardware structure for storing the indicator elements enforcing a requirement that the memory regions be necessarily disjoint, the modifiable indicator elements each having a value indicating the architecture and data storage convention under which instructions from the associated region are to be executed;
>
> when execution of the instruction data flows or transfers between the first, second and third regions, adapting the computer for execution in the architecture and/or convention of the region transferred to.

Claim 104 recites two memory regions that "[follow] first and second data storage conventions." As discussed above in connection with claim 22, at page 34, there is no indication that Goetz '913 uses two different "data storage conventions." Indeed, it appears that Goetz deliberately avoids this. Accordingly, claim 104 is not anticipated by Goetz '913.[2]

Claim 113 recites similar limitations and is patentable for similar reasons.

IX. Dependent claims

The dependent claims are patentable with the independent claims discussed above. In addition, the dependent claims recite additional features that further distinguish the art.

X. Claim Amendments

In this Response, claim 63 is rewritten into independent form by incorporating the limitations of its parent claims. Thus, this amendment is not made for a substantial reason related to patentability. Further, claim 63 is an "unamended claim" for purposes of final rejection practice under MPEP § 706.07(a), and for purposes of claim interpretation.

XI. Conclusion

In view of the amendments and remarks, Applicant respectfully submits that the claims are in condition for allowance. Applicant requests that the application be passed to issue in due course. The Examiner is urged to telephone Applicant's undersigned counsel at the number noted below if it will advance the prosecution of this application, or with any suggestion to resolve any condition that would impede allowance. Enclosed is a Petition for Extension of

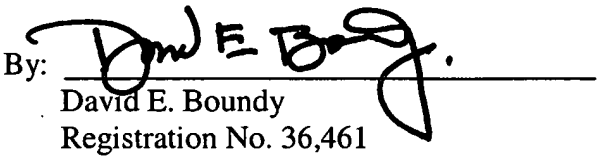
[2] Applicant notes that claim 104 recites two memory regions that are "necessarily disjoint." Claims 104 and 113 are the only two claims that recite this limitation. Paragraph 42 of the Office Action does not mention this limitation, or state where "the same reasons set fourth [sic] in the previous claim rejections, supra" can be found. Thus, paragraph 42 is insufficient to state any rejection of these claims.

Time for two months. In the event that any further extension of time is required, Applicant petitions for that extension of time required to make this response timely. Kindly charge any additional fee, or credit any surplus, to Deposit Account No. 23-2405, Order No. 114596-03-4000.

Respectfully submitted,

WILLKIE FARR & GALLAGHER, LLP

Dated: July 12, 2004

By: 

David E. Boundy
Registration No. 36,461

WILLKIE FARR & GALLAGHER, LLP
787 Seventh Ave.
New York, New York 10019
(212) 728-8000
(212) 728-8111 Fax

3. For non-patent items listed on the enclosed Form PTO-1449 for which a copy is not already made of record in this application, a copy was previously cited by or submitted to the Patent and Trademark Office in application Serial No. 09/239,194, filed January 28, 1999, Yates et al., Executing Programs for a First Computer Architecture on a Computer of a Second Architecture, in application Serial No. 09/322,443, filed May 28, 1999, Reese et al., Profiling of Computer Programs Executing in Virtual Memory Systems, or in application 09/626,325, filed July 26, 2000, Yates, et al., Computer with Two Operating Systems.

4. This Information Disclosure Statement is being filed more than three months after filing of this application and after the mailing of a first Office Action on the merits, but before the mailing date of a final action under 37 C.F.R. § 1.113, or a Notice of Allowance under 37 C.F.R. § 1.311 (where there has been no prior final action), or an action that otherwise closes prosecution in the application. A fee is due pursuant to 37 C.F.R. §1.97(c)(2).

5. A check in the amount of $ 180.00 is enclosed in payment of the fee due under C.F.R. §1.17(p).

6. The Commissioner is hereby authorized to charge any additional fees that may be required for this Information Disclosure Statement, or credit any overpayment, to Deposit Account No. 23-2405, Order No. 114596-03-4000.

Respectfully submitted,
WILLKIE FARR & GALLAGHER, LLP

Dated: July 12, 2004

By: _____
David E. Boundy
Registration No. 36,461

WILLKIE FARR & GALLAGHER, LLP
787 Seventh Ave.
New York, New York 10019
(212) 728-8000
(212) 728-8111 Fax